REMARKS

The Office Action dated July 27, 2005, has been received and carefully considered. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Allowability of Claim 7

The Applicant notes with appreciation the indication at pages 13 and 14 of the Office Action that claim 7 is allowed.

Obviousness Rejection of Claims 1-5, 8-10 and 19-21

At page 2 of the Office Action, claims 1-5, 8-10 and 19-21 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang (U.S. Application Publication No. 2003/0005247) in view of Hahm (U.S. Patent No. 6,233,646). This rejection is hereby respectfully traversed.

Claim 1, from which claims 2-6 and 8-10 depend, and claims 19 and 21 recite the features of when in a first mode of operation, utilizing a first output coupled to a memory to provide a first data lane enable for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address and when in a second mode of operation, *utilizing the first output to provide an address bit of a second memory address* for *facilitating designation of a second memory storage location of the memory*. With respect to these features, the Office Action asserts that Chang discloses a memory access system having a first mode of operation, "facilitating access of a portion of a first memory storage location associated with a first memory address within the 1Mbytes address range," citing claim 1 and page 1, paras. 5-8. Additionally, the Office Action asserts that Change discloses "a second mode of operation" that utilizes the first output "to provide an address bit of a second memory address" (referring to output link from CPU 200 to memory 240) "for faciliting designation of a second memory storage location (addressing range beyond 1 Mbyte) of the memory." (*see Office Action*, pp. 2-3). The Office Action then concludes that "[s]ince the SMM allows for normal access of this addressing range by the SMI, the access is completed through the use of address bits identifying the memory address to be accessed." (*see Office Action*, p. 3).

The Office Action acknowledges that

> Chang does not teach using a first output coupled to the memory to provide a first data lane enable for facilitating access of a portion of a first memory storage location associated with a first memory address.

Office Action, p. 3. However, the Office Action instead improperly relies on Hahm as allegedly disclosing

> a first output (Figure 1, "enable" output from External Memory Address and Control Signal Generator 7) coupled to the memory 300 to provide a data lane enable ("enable" signal) for facilitating access (controlling read and write operation of the data, see Figure 1 and Col. 3, lines 15-16 and 28-35, and Col. 4, lines 34-40) of a portion of a first memory 300 storage location associated with a memory address ("address (19)" output from External Memory Address and Control Signal Generator 7).

Office Action, p. 3. The Office Action then concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CPU-based memory control of Chang "to employ the use of the memory interface controller 100 of Hahm when performing memory accesses since the memory interface controller takes full control of read and write access operations (Column 3, lines 5-35) thus, allowing for the CPU to dedicate its resources to other processes." *See Office Action*, p. 3.

Contrary to the assertions contained in the Office Action, the Applicants respectfully submit that the proposed combination of Chang and Hahm fail to teach, suggest or disclose each and every element recited by claims 1-5, 8-10 and 19-21. Moreover, the cited combination does not result in the invention as recited in the claims. Finally, there is no suggestion and no motivation for modifying the teachings of Chang in view of Hahm as proposed by the Office Action.

1) Chang and Hahm Fail to Disclose or Suggest an Output that Provides a Data Lane Enable in a First Mode and an Address Bit in a Second Mode

The Office Action states that Hahm "discloses a first output" (an "enable" output from External Memory Address and Control Signal Generator 7) that is analogous to the first output of claim 1. *See Office Action*, p. 3. As provided in claims 1, 19 and 21, the first output is utilized to provide a first data lane enable in a first mode and to provide an address bit in a second mode.

By contrast, the "enable" signal of Hahm only specifies a mode of operation (i.e. read, write, Daisy chain, 16-bit, and so on). Specifically, the Hahm reference discloses a "read enable signal RD, a write enable signal WR, a Daisy-chain enable signal and an enable signal in accordance with a 16-bit sequence number SN 16." *See* Col. 3, lines 9-12 and FIG. 2. Additionally, Hahm discloses

> an extended memory address and control signal generator for generating an address 19 and a control signal (read/write/enable) and outputting to the RAM 200 and the extended ram 300 in accordance with a read enable signal RD, a write enable signal WR, a priority match address, and extended memory empty flag address and an extended memory flag address from the control logic unit 1.

See Col. 4, lines 33-40. In contrast to the embodiments recited in claims 1, 19 and 21, the enable signal of Hahm is not utilized to provide a first data lane enable in a first mode *and to provide an address bit in a second mode*. Instead, the enable signal of Hahm specifies only the mode of operation, and does not provide an address bit of a second memory address in a second mode of operation as asserted in the Office Action. Hahm provides no disclosure or suggestion that the enable signal can be used to provide an address bit of a memory address designating a memory storage location of a memory. Thus, Hahm does not suggest or disclose a first output coupled to the memory to provide a data lane enable in a first mode of operation and to provide an address bit of a second memory address for a second memory storage location of the memory as recited in claims 1, 19 and 21.

The SMI signal of Chang is a system management interrupt (SMI) signal that is provided by the chipset 220 (Chang, FIG. 2) to the CPU 200 (Chang, FIG. 2) in order to direct the CPU 200 to enter the system management mode (SMM) and to actuate a SMI handler routine. *See Chang*, para. 0031. Thus, Chang teaches the use of the SMI signal to trigger the initiation of the SMM and SMI hander routine at the CPU 200. Chang, however, does not disclose or even suggest that the SMI signal is used to provide an address bit as recited. Accordingly, the proposed combination of Chang and Hahm fails to disclose or suggest the features of utilizing a first output to *provide a first data lane enable* for facilitating access of a portion of a first memory location when in a first mode and utilizing the first output to *provide an address bit* of a second memory address when in a second mode as recited by claims 1, 19 and 21.

2) The Proposed Modification of Chang in view of Hahm Does Not Result in the Embodiment of the Invention as Recited in Claims 1, 19 and 21

The Office Action asserts that

> it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang to employ the use of the memory interface controller 100 of Hahm when performing memory accesses since the memory interface controller [100] takes full control of read and write access operations (Column 3, line 5-35) thus, allowing for the CPU to dedicate its resources to other processes.

Office Action p. 3. The Applicants respectfully submit that the mere integration of the components of the system of Chang into a single device would not affect the interconnection of the components and therefore would not result in the SMIOUT# pin (which provides the SMI signal) being coupled to the memory 140. Instead, the SMIOUT#pin of Chang would couple to the memory interface controller 100 of Hahm, which is in turn coupled to the memory. The combined structure does not result in *a first output coupled to a memory* as recited by claims 1, 19 and 21.

Additionally, it is not clear from the references or from this assertion how such a combination might work. For example, the alleged second mode of operation of Chang employs a system management interrupt (SMI) signal to initiate a System Management Mode (SMM) and to initiate an SMI handler routine, which is able to access the memory space identified by addresses in a range beyond than 1 Mbytes. *See Chang*, p. 2, paras. 0031 and 0033. By contrast, the memory interface controller 100 of Hahm generates an enable signal for specifying a mode of operation, not a second memory address. Consequently, the resulting combination would lead to the SMI signal and resultant SMI handler routine being received by the memory interface controller 100 of Hahm. This is not a *first output coupled to a memory* as recited in claims 1, 19 and 21, and this does not equate to a *first output to provide an address bit of a second memory address* in a second mode of operation, as recited by claims 1, 19 and 21. Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm fails to disclose or suggest all of the elements of claims 1, 19 and 21.

3) There is No Motivation to Combine Chang and Hahm

Not only does the proposed combination of Chang and Hahm fail to disclose or suggest features of claim 1, but there is no motivation to combine the teachings of Chang and Hahm. The Office Action asserts that the alleged combination is motivated by a desire to free up the CPU for other processes. Specifically, the Office action states that the interface controller of Hahm "takes full control of read and write access operations," "thus, allowing for the CPU to dedicate its resources to other processes." *See Office Action*, p. 3. However, this assertion is unsupported by the cited references, and there is no indication that the resultant combination would free up the CPU of Chang. As discussed above, the SMI signal of Chang is a software interrupt or enable signal that is used to direct the CPU 200 of Chang to enter the SMM mode and to initiate a SMI interrupt handler routine. Hahm merely provides a memory interface that can be integrated into a field programmable gate array (FPGA) and provides no disclosure or suggestion that a system interrupt signal that is provided to a CPU, such as the SMI signal of Chang, also may be provided to a memory. Nor does it provide any instruction as to how the system interrupt signal might be used by the memory.

Additionally, Chang makes no reference to a desire to free up the CPU for other processes, but rather uses the interrupt to halt the CPU operation to perform memory access. Hahm makes no reference to system interrupts. In particular, Chang teaches a system having a CPU 200 connected to a memory 240, where the CPU 200 receives a SMI signal from a chipset 220. By contrast, Hahm discloses a Field Programmable Gate Array (FPGA) that can operate as a memory controller interface 100. One of ordinary skill in the art will appreciate that a conventional FPGA cannot implement a CPU. Consequently, Hahm teaches away from the incorporation of the system of Chang into a single device.

Thus, the asserted basis for making the combination does not derive from the teachings of the Chang or the Hahm references. Instead, the asserted combination constitutes a hindsight reconstruction based on the present disclosure.

The asserted combination fails to disclose all the elements of independent claims 1, 19 and 21. Therefore, the rejections of claims 1, 19 and 21 over the combination of Chang and Hahm are improper and should be withdrawn. Consideration and notice to that effect is respectfully requested.

Claims 2-5 and 8-10 depend from independent claim 1 and claim 20 depends from independent claim 19. Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm does not disclose or suggest each and every feature of claims 2-5, 8-10 and 20 at least by virtue of their dependency from claims 1 and 19. Moreover, these claims recite additional features neither disclosed nor suggested by Chang or Hahm. Consequently, it is respectfully submitted that the obviousness rejections of claims 1-6, 8-10 and 20 are improper at this time, and withdrawal of these rejections therefore is respectfully requested. Consideration and notice to that effect is respectfully requested.

Obviousness Rejection of Claims 16-18

At pages 4 through 7 of the Office Action, claims 16 and 18 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang (U.S. Application Publication No. 2003/0005247) in view of Hahm (U.S. Patent No. 6,233,646). At page 13, claim 17 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm and further in view of the Authoritative Dictionary of IEEE Standard Terms. This rejection is hereby respectfully traversed.

1) Chang and Hahm Fail to Disclose or Suggest an Output that Provides a Data Lane Enable in a First Mode and an Address Bit in a Second Mode

Independent claim 16 reads as follows:

16. (Previously Presented) An apparatus comprising:

a first register having an output to indicate one of a first mode of operation and a second mode of operation;
an address control portion having an input coupled to the output of the first register, and an output to indicate a value of an address bit when in the first mode of operation;
a first data lane enable control portion having an input coupled to the output of the first register, and an output to indicate a first data lane enable value when in the second mode of operation; and
an output pin coupled to the output of the address control portion and the output of the first data lane enable control portion, and further coupled to a memory.

The Office Action asserts that Chang shows "a first register (real mode register 100 within CPU 200) having an output to indicate one of a first mode of operation and a second mode of operation." *Office Action*, p. 5. However, the "real mode 100" in Chang is not indicated to be a

register, but rather a mode of operation. For example, "[a]s shown in FIG. 1, if the CPU currently operates under the *real mode* 100, the CPU needs to be switched into the *protected mode* 120 before accessing memory 140 at a location greater than the standard 1 Mbytes memory space." *See Chang*, p. 1, para. 0006. Consequently, real mode 100 does not equate to a first register as suggested in the Office Action.

The Office Action asserts that the software interrupt request equates to a second mode of operation, and that the software interrupt interface 160 equates to "an address control portion" "having an input coupled to the output of the first register (Real Mode Register 100) and an output to indicate a value of an address bit when in the first mode of operation." However, as discussed above, the real mode 100 is not indicated by Chang to be a register, but rather a mode of operation.

The Office Action acknowledges that Chang does not teach a first data lane enable control portion, but points to the enable signal of Hahm for this element. However, the cited combination does not teach all the elements of claim 16.

Claim 16 recites a first data lane enable control portion *having an input coupled to the output of the first register*, and *an output to indicate a first data lane enable value* when in the second mode of operation. Claim 16 further recites an *output pin coupled to the output of the address control portion and the output of the first data lane enable control portion, and further coupled to a memory*. Chang and Hahm do not teach, suggest or disclose either of these elements, and they do not disclose the first register or the address control portion elements recited in claim 16. Chang and Hahm fail to disclose or suggest an output pin coupled to the output of the address control portion, as recited in claim 16. As further provided by claim 16, the output pin is also coupled to the output of the first data lane enable control portion that is to indicate a first data lane enable value when in the second mode of operation. In contrast, and as noted above, the SMI signal of Chang is a system management interrupt (SMI) signal that is provided by the chipset 220 (Chang, FIG. 2) to the CPU 200 (Chang, FIG. 2) in order to direct the CPU to enter the system management mode (SMM) and to actuate an SMI handler routine. *See* Chang, para. 0031. Chang does not disclose or suggest that the SMI signal is used to indicate the value of an address bit. Hahm does not suggest or disclose that system interrupt signals provided to a CPU, such as the SMI signal of Chang, are used to provide an address bit of a memory address designating a memory storage location of a memory. The Office Action fails

to demonstrate that Chang and Hahm suggest or disclose all the elements of claim 16. Therefore, the rejection of claim 16 is improper, and withdrawal of the rejection is respectfully requested.

2) There is No Motivation to Combine Chang and Hahm

In addition, for at least the reasons presented above in reference to claims 1 and 21, there is no teaching or suggestion to combine the Chang and Hahm references, and the resulting combination does not achieve the embodiment recited in claim 16. Consequently, the asserted motivation to combine the inventions of Chang and Hahm constitutes a hindsight reconstruction based on the present disclosure, and the resulting combination does not result in the particular combination of features as recited in claim 16. Thus, the rejection of claim 16 over the combination of Chang and Hahm is improper and should be withdrawn. Consideration and notice to that effect is respectfully requested.

3) There is No Motivation to Combine Chang, Hahm and the Authoritative Dictionary of IEEE Standard Terms

At page 13 of the Office Action, claim 17 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm and further in view of Authoritative Dictionary of IEEE Standard Terms. This rejection is hereby respectfully traversed.

Claim 17 depends from claim 16. As previously discussed, the combination of Chang and Hahm do not disclose or suggest each and every feature of claim 16, as well as each and every feature of claim 17 at least by virtue of their dependency from claim 16. The Office Action at page 13 acknowledges that Chang in view of Hahm "does not teach a multiplexor used to transmit a number of inputs to the address control portion while supplying one output." However, the Office Action states

> in systems where a selection is being made from two modes of operations, it is common to use a multiplexor to enable the selection (see IEEE Dictionary, Page 716). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a multiplexor in the system of Chang for selection purposes since a multiplexor enables for quick selections (see term definition).

See Office Action, p. 13. However, contrary to the assertions of the Office Action, the Applicants respectfully submit that the proposed combinations of Chang, Hahm and the Authoritative Dictionary of IEEE Standard Terms (the "IEEE dictionary") fail to disclose or suggest each and every feature recited by claims 16 and 17, and further submit that there is no

motivation to modify the teachings of Chang in view of Hahm and in view of the IEEE dictionary.

As previously discussed, Chang and Hahm fail to disclose or suggest an output pin coupled to an output of an address control portion that is to indicate a value of an address bit when in a first mode and an output of a first data lane enable control portion to indicate a first data lane enable when in a second mode as recited by claim 16. Moreovér, the proposed combination of Chang and Hahm fails to disclose or suggest the features of the output pin being coupled to a memory as recited by claim 16. The Office Action does not assert that the IEEE Dictionary discloses or suggests these features. In view of the foregoing, it is respectfully submitted that the Office Action fails to establish that Chang, Hahm and the IEEE Dictionary disclose or suggest, alone or in combination, each and every feature of claim 17.

Claim 18 depends from independent claim 16. Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm does not disclose or suggest each and every feature of claim 16, as well as each and every feature of claims 17 and 18 at least by virtue of their dependency from claim 16. Moreover, claims 17 and 18 recite additional features neither disclosed nor suggested by Chang or Hahm. Specifically, the feature as recited in claim 16 *wherein the first register is associated with one of a plurality of chip selects* is not suggested or disclosed by the cited references, either alone or in combination. Consequently, it is respectfully submitted that the obviousness rejections of claims 16-18 are improper at this time, and withdrawal of these rejections therefore is respectfully requested. Consideration and notice to that effect is respectfully requested.

Obviousness Rejection of Claims 6, 11-15, and 20

At pages 7-13 of the Office Action, claims 6, 11-15 and 20 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm and further in view of Microsoft Computer Dictionary. This rejection is hereby respectfully traversed.

1) Chang, Hahm and the Microsoft Computer Dictionary Fail to Disclose or Suggest a Third Mode

Claim 6 depends from claim 1 and claim 20 depends from claim 19. As previously discussed, the cited art does not suggest or disclose all the elements of claims 1 and 19. Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm does

not disclose or suggest each and every feature of claims 1 and 19, as well as each and every feature of claims 6 and 20 at least by virtue of their dependency from claims 1 and 19. Moreover, these claims recite additional features neither disclosed nor suggested by Chang or Hahm. Specifically, the third mode of operation is not disclosed by either the Chang or Hahm references.

Claims 6 and 20 recite a third mode of operation. The Office Action asserts that computer systems "are known to have internal primary storage for their direct access (Main Memory, see Microsoft Computer Dictionary, Page 355)." *Office Action*, p. 7. Moreover, the Office Action states

> it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation tracking internal primary storage access (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage.

Office Action, p. 7. However, even if such internal primary storage was known as asserted by the Office Action, the existence of such internal storage does not provide motivation for the modification of Chang, and does not render obvious such "integration." In particular, the Chang reference utilizes a system management interrupt signal to switch between "real mode 100" and "protected mode 120". *See* FIG. 1 and FIG. 3, *and see* p. 3, para. 0033. It is unclear how such a third addressing range would be implemented in Chang. Chang and Hahm do not provide any suggestion of a third mode of operation or a third memory range, and they do not provide any indication of how a third addressing range could be implemented.

Consequently, it is respectfully submitted that the obviousness rejections of claims 6 and 20 are improper at this time, and withdrawal of these rejections therefore is respectfully requested. Consideration and notice to that effect is respectfully requested.

2) There is No Motivation to Combine Chang, Hahm and the Microsoft Computer Dictionary

Independent claim 11 reads as follows:

> 11. (Previously Presented) A method of providing data to a set of pins of a device, the set of pins coupled to a memory, the method comprising:
> during a *first mode of operation, multiplexing a first set of data onto the set of pins to allow the set of pins to provide data representing two least significant bits of a first address*, a most significant bit of the first address, and a lane enable;

during *a second mode of operation, multiplexing a second set of data onto the set of pins to allow the set of pins to provide data representing one least significant bit of a second address, a most significant bit of the second address, and two lane enables*; and
during a *third mode of operation, multiplexing a third set of data onto the set of pins to allow the set of pins to provide four lane enables*.

The combination of Chang and Hahm do not suggest or disclose a first mode of operation and a second mode of operation wherein the set of pins provide data representing two least significant bits and a most significant bit of a first address in a first mode and data representing one least significant bit and a most significant bit of a second address in a second mode. Additionally, neither Chang nor Hahm suggest or disclose allowing the set of pins to provide a lane enable in a first mode of operation, two lane enables in a second mode of operation, and four lane enables in a third mode of operation. Additionally, neither reference makes any mention of a third mode of operation.

The Office Action asserts, as before, that the Microsoft Computer Dictionary shows that internal primary storage for direct access is known with regard to "Main Memory", and that

> it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into the system of the combination of Chang in view of Hahm the use of a third mode of operation tracking internal primary storage accesses (third accessing range), thus allowing the system to more accurately monitor accesses to all available storage. Since the modified system of Chang in view of Hahm only has two modes of operation, only one lane enable is necessary for its operation. However, it is understood that in adding another mode of operation more lane enables and chip selects are needed in order to differentiate between operation modes and addressing ranges.

Office Action, p. 9. As previously discussed, it is unclear how such a third mode could be implemented in a system combining Chang with Hahm, but such a system could not be implemented without modifying Chang's system management interrupt system away from its current implementation. There is no teaching in any of the cited references motivating such a modification.

As previously discussed, there is no suggestion or motivation within the cited references to make the combination asserted in the Office Action. The only basis for making such a combination is provided by the present disclosure and by the elements recited in the claims. Consequently, the asserted motivation constitutes a hindsight reconstruction based on the present disclosure. Therefore, the rejection of claim 11 over the combination of Chang, Hahm and

Microsoft Computer Dictionary is improper, and should be withdrawn. Consideration and notice to that effect is respectfully requested.

Claims 12-15 depend from claim 11. Accordingly, it is respectfully submitted that the proposed combination of Chang, Hahm, and page 355 of the Microsoft Computer Dictionary do not disclose or suggest each and every feature of claim 11, as well as each and every feature of claims 12-15 at least by virtue of their dependency from claim 11. Moreover, claims 12-15 recite additional features neither disclosed nor suggested by Chang, Hahm, or the Microsoft Computer Dictionary. Consequently, it is respectfully submitted that the obviousness rejections of claims 11-15 are improper at this time, and withdrawal of these rejections therefore is respectfully requested. Consideration and notice to that effect is respectfully requested.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

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Date

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